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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/787,290	06/28/2001	Jonathan Westphal	52254-016	6488

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EXAMINER	
STEVENS, THOMAS H	

ART UNIT	PAPER NUMBER
2121	

MAIL DATE	DELIVERY MODE
07/03/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/787,290	WESTPHAL, JONATHAN	
	Examiner	Art Unit	
	Thomas H. Stevens	2121	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-12 were examined.

Section I: Final Rejection

Specification

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-7 rejected under 35 U.S.C. 103(a) as being unpatentable over applicants own admission (i.e., specification (AOA)) in view of Pillage et al., (US Application 5,379,231) (hereafter Pillage). AOA and Pillage are analogous since they both teach logic circuits.

((AOA) as set forth above generally discloses the basic inventions.)

Regarding claims 1,2,5

AOA teaches,

- simpler form (AOA, specification, pg. 24, 3rd paragraph with 4th paragraph, lines 4 and 5 "logical device" "simplification machine")
- vector space (pg.24, summary of invention, line 7)

AOA fails to teach logic circuits as well as designing logic circuits.

Pillage teaches,

- designing logic circuits (Pillage: column 1, lines 6 and 7),
- logic circuit (Pillage: column 5, lines 3-5)

Therefore it would have been obvious to one having ordinary skill in the art at the time of invention was made to utilize the logic devices of Pillage in the vector analysis of AOA because Pillage teaches a method to provide an improved method and apparatus for simulating behavior of a microelectronic interconnect circuit at higher speeds than conventional circuit simulators (Pillage: column 3, lines 19-21).

Regarding claim 3,

Pillage teaches,

- modifying (Pillage: column 42, lines 43-44)
- using at least one process rule of a set of process rules (series of steps, thus imply a series of rules: Pillage: column 34, lines 25 and 26)

Regarding claim 4,

- at least one process rule of a set of process rules consisting of one of the following process rules: comprising the steps of representing in alternational normal schema; a target schema **t**, as a set of vectors in ANS-space; each vector clause or disjunct of **t** is a position vector with a **O** at one corner of a set of parallelograms made of propositional addresses to the I-point at the other; any two other outside vertices of such a parallelogram are implicants of **t** (AOA, specification: 11, paragraphs 1-2 and 6).

Regarding claim 6,

AOA teaches,

- an optical computer (AOA: pg. 24, paragraphs 3-4).

Regarding claim 7,

- a digital computer (AOA: pg. 1, "Description of Related Art" section, line 11 "Digital computers are, of course, well-known.").

5. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Pillage in view of AOA as applied to claim 5 above, and further in view of Chan et al., (US Patent 6,262,812) (hereafter Chan).

Regarding claim 8,

Pillage teaches, designing logic circuits (Pillage: column 1, lines 6 and 7)

Chan teaches a colorimetric computer (Chan: column 3, lines 46-48) to maximize the dynamic range of image values output from the image adjustment system (Chan: column 1, lines 50-52).

6. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Pillage in view of AOA as applied to claim1 above, and further in view of Yount (US Patent 4,622,667).

Regarding claim 9,

Pillage teaches, designing logic circuits (Pillage: column 1, lines 6 and 7),

Yount teaches an analog computer (Yount: column 2, line 16) to reduce safety hazards resulting from generic faults in the software or the processors (Yount: column 1, lines 10-12)

7. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pillage in view of AOA and further in view of Eng (US Patent 6,145,117).

Regarding claims 10-12,

Pillage teaches, designing logic circuits (Pillage: column 1, lines 6 and 7)

Eng teaches memory (Eng: column 12, lines 31-32) and computer program (Eng: column 25, line 37) enhances existing top-down EDA systems by implementing an automatic performance design paradigm (Eng: column 3, lines 38-40).

Section II: Response to Arguments

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8. Applicants are thanked for responding to this issue. Applicant are correct in that there was never an objection to claims 3,4,5,8 and 9 to which the Examiner believes the applicant meant to say "rejections" to claims 3,4,5,8 and 9 (claim 3 is mentioned since its dependence are referred to claim 3). The rejections to these claims are withdrawn.

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9. The examiner fails to comprehend Applicant's confusion of the rejection. Simply put, both pieces of art are analogous since they teach digital logic circuits. Applicants are conducting piecemeal analysis in their arguments; one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In this instance, aside from the fact that vector spaces are known mathematical functions, Pillage does mention vector spaces (column 21, line 4, "vector in the space"). Applicants are correct in denoting Pillage's lack of teaching simplifying logic; however,

AOA teaches this limitation in their description of related art section which discusses the "desire to reduce the number of complements required for performing a particular logic function or sets of functions" (pg. 1, lines 8-9). This limitation is considered prior art since it's mentioned as related art and the science of circuit reduction is well known.

Applicant states their concern whether the Examiner's explanation of Applicant's admission of prior art (Applicant's response, pages 18 and 19). **The Examiner's rationale is that both pieces of art are analogous to the teaching of logic circuits. Secondly, it apparent that the source of the claim language stems from sections of the National Academy of Sciences Panel of Photonics (1988), which is dated material i.e., prior art.**

Applicant states there's no prima facie case of obviousness. Conversely, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize the optical computers of AOA in the design and manufacturing of Pillage since AOA teaches a method in which optical computers can perform the same functions performed by digital computers but in a principle much faster (AOA: page 1, lines 12-14). **Furthermore, a person with a master's level in the art would be familiar with the transfer of properties of linear algebra into logic gate reduction thus reflecting no material change.**

10. Applicant's arguments filed on 09/22/2006 have been fully considered but they are not persuasive. In response to applicant's argument that the Examiner has not shown why it would have been obvious to adapt information from a patent on a

computer printing system...etc.", the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

The Examiner is unclear to applicant's arguments on page 23, paragraphs 1 and 2 regarding the use of the Yount reference since there's no redundant data reference mentioned in claim 9 and the examiner has never requested to withdraw the rejection.

Applicant's query to the use of Eng coupled with the prior art by Pillage and AOA. As mentioned in the previous office action, all three pieces of art are analogous to logic circuits. Eng is used since it teaches computer programming with memory. The rejections as set forth above stand.

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

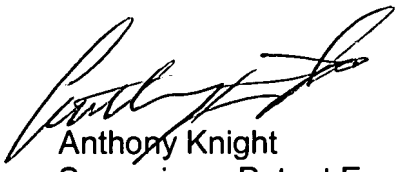
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Correspondence Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mr. Tom Stevens whose telephone number is 571-272-3715.

If attempts to reach the examiner by telephone are unsuccessful, please contact examiner's supervisor Mr. Anthony Knight 571-272-3687. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov.. Answers to questions regarding access to the Private PAIR system, contact the Electronic Business Center (EBC) (toll-free (866-217-9197)).



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